Amendments to the Claims

Please amend Claims 9 and 13. Please add new claims 16-19. The Claim Listing below will replace all prior versions of the claims in the application:

Claim Listing

1. (Original) A delay locked loop comprising:

a delay circuit which provides a delay to a reference clock to generate a feedback clock, the delay circuit having a delay range;

a phase detector which compares phase of the reference clock and the feedback clock to change the delay of the delay circuit; and

an initialization circuit that after reset of the delay locked loop assures that the phase detector initially changes the delay in a direction away from a first end of the delay range after receipt of one of the reference clock and feedback clock and enables a change in the delay in an opposite direction toward the first end only after receipt of one of the reference clock and feedback clock followed by receipt of the other of the reference clock and feedback clock.

2. (Original) The delay locked loop of claim 1 wherein the first end of the delay range is a minimum delay and the direction away from the first end increases the delay and the opposite direction towards the first end decreases the delay.

3. (Original) The delay locked loop of claim 2 wherein the initialization circuit increases the delay after receipt of the reference clock and enables decrease in the delay only after receipt of the reference clock followed by the feedback clock.

4. (Original) The phase detector of claim 1 wherein the initialization circuit comprises:

a first latch responsive to the reference clock which detects a first edge of the reference clock to enable change in the delay in the direction away from the first end; and

a second latch responsive to the feedback clock which detects an edge of the feedback clock after the first edge of the reference clock has been detected by the first

latch to enable change in the delay in the opposite direction, the input of the second latch coupled to the output of the first latch.

5. (Original) The phase detector of claim 4 wherein the initialization circuit further comprises:

a third latch responsive to the reference clock which detects a next edge of the reference clock to delay enabling change in the delay in the first direction for at least one reference clock period, the input of the third latch coupled to the output of the first latch; and

a fourth latch responsive to the feedback clock which detects a next edge of the feedback clock to delay the enabling of change in the delay in the opposite direction for at least one feedback clock period, the input of the fourth latch coupled to the output of the third latch.

6. (Previously presented) The phase detector as claimed in claim 4 wherein the first edge of the reference clock is a rising edge and the edge of the feedback clock is a rising edge.

7. (Original) The phase detector of claim 1 wherein the initialization circuit comprises:

a first latch responsive to the feedback clock which detects a first edge of the feedback clock to enable change in the delay in the direction away from the first end; and

a second latch responsive to the reference clock which detects an edge of the reference clock after the first edge of the feedback clock has been detected by the first latch to enable change in the delay in the opposite direction, the input of the second latch coupled to the output of the first latch.

8. (Original) The delay locked loop of claim 1 wherein the phase detector comprises:

a latch responsive to the reference clock to generate a first phase control signal; and

another latch responsive to the feedback clock to generate a second phase control signal.

9. (Currently amended) A method for initializing a delay locked loop comprising the steps of:

providing a delay to a reference clock to generate a feedback clock, [[the]] a delay circuit providing the delay being initially set at a first end of a delay range;

comparing phase of the reference clock and the feedback clock to change the delay of the delay circuit;

after reset of the delay locked loop assuring that the delay initially be changed in a direction away from the first end of the delay range after receipt of the reference clock; and

enabling a change in the delay in an opposite direction toward the first end only after receipt of the reference clock followed by receipt of the feedback clock.

10. (Original) The method of claim 9 wherein the first end of the delay range is a minimum delay and the direction away from the first end increases the delay.

11. (Previously presented) The method of claim 9 further comprising the steps of:

delaying enabling adjustment of the delay in the direction away from the first end until a first predetermined number of reference clock edges are detected; and

delaying enabling adjustment in the opposite direction until a second predetermined number of the reference clock edges are detected.

12. (Previously presented) The method of claim 11 wherein the reference clock edges are rising edges.

13. (Currently amended) A delay locked loop comprising:

means including a delay circuit for providing a delay to a reference clock to generate a feedback clock, the delay circuit being initially set at a first end of a delay range;

means for comparing phase of the reference clock and the feedback clock to change the delay of the delay circuit; and

after reset of the delay locked loop means for assuring that the delay initially be changed in a direction away from the first end of the delay range after receipt of the reference clock; and

means for enabling a change in the delay in an opposite direction toward the first end only after receipt of the reference clock followed by receipt of the feedback clock.

14. (Original) A phase detection circuit for comparing phase of a first and second input signals comprising:

a first latch responsive to the first input signal to generate a first phase control signal;

a second latch responsive to the second input signal to generate a second phase control signal;

an initialization circuit that enables the first latch after receipt of one of the first and second input signals and enables the second latch only after receipt of the one of the first and second input signals followed by receipt of the other of the first and second input signals.

15. (Original) The phase detection circuit of claim 14, wherein the initialization circuit enables the first latch after receipt of a first plurality of said one of the first and second input signals and enables the second latch only after enabling the first latch and the receipt of a second plurality of said other of the first and second input signals.

16. (New) The delay locked loop of claim 1, further comprising a reset circuit controlling the reset of the delay locked loop in response to a reset signal, the initialization circuit resetting in response to the reset signal.

17. (New) The method of claim 9, further comprising controlling the reset of the delay locked loop in response to a reset signal.

18. (New) The delay locked loop of claim 13, further comprising means for controlling the reset of the delay locked loop in response to a reset signal.

19. (New) The phase detection circuit of claim 14, further comprising a reset circuit controlling the reset of the delay locked loop in response to a reset signal, the initialization circuit resetting in response to the reset signal.